CLAIMS

1. A memory cell, comprising:

a charge storage element;

a one-transistor switch constructed and arranged to selectively connect the storage element to a first data line, responsive to a first select signal; and

a one-transistor gain element having an input connected to receive a signal from the storage element and constructed and arranged to selectively provide a corresponding output signal to a second data line, responsive to a second select signal.

2. The memory cell of claim 1, wherein the switch is an FET having a drain connected to the first data line, a source connected to the storage element and a gate connected to the first select signal.

3. The memory cell of claim 2, wherein the gain element is an FET having a gate connected to the storage element, a source connected to the second data line and a drain selectively connected to one of a first power supply and a second power supply.

4. The memory cell of claim 2, wherein the switch transfers a signal from the first data line onto the storage element and transfers a signal from the storage element onto the first data line when selected by the first select signal.

5. A two-dimensional array of memory cells, comprising:

a first select signal line running through the array in a first direction;

a second select signal line running though the array in a second direction;

first and second data lines; and

each cell having

a charge storage element,

a one-transistor switch constructed and arranged to selectively connect the storage element to the first data line responsive to a first select signal, and

a one-transistor gain element having an input connected to receive a signal from the storage element and constructed and arranged to selectively provide a corresponding output signal to a second data line, responsive to a second select signal.

6. A method of addressing an array of memory cells, comprising:

writing groups of bits linearly arrayed with respect to each other; and

reading groups of bits linearly arrayed with respect to each other and orthogonally disposed to the groups of bits written.